

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1 (Cancelled):

Claim 2 (Previously Presented):

2 The electronic circuit as recited in claim 3, wherein when the self-test
3 detects that one of the slice arrays is defect free, the remap register
4 associated with that slice array is set to indicate that the slice array is
5 defect free resulting in the associated remap selector circuit instructing
6 the associated write selector circuit to direct data intended for storage
7 in that slice array to that slice array and instructing the associated read
8 selector circuit to direct data read from that slice array to the output of
9 that slice array.

Claim 3 (Previously Presented):

2 An electronic circuit for self-repair of a random access memory array,
3 comprising:
4 a write selector circuit associated with each slice array, wherein the
5 random access memory is organized into a plurality of slice arrays,
6 wherein each slice array comprises at least one memory storage cell,
7 and wherein at least one of the slice arrays is redundant;
8 a read selector circuit associated with each slice array;
9 a remap selector circuit associated with each slice array; and
10 a remap register associated with each slice array, wherein when power
11 is applied to the circuit, the circuit automatically performs a self-test,
12 wherein when the self-test detects a defect, the remap register of the
13 slice array having the defect is set to indicate the presence of the defect
14 resulting in the associated remap selector circuit instructing the
15 associated write selector circuit to redirect data intended for storage in
16 that slice array to an adjacent slice array and instructing the associated
17 read selector circuit to redirect data read from the adjacent slice array
18 to the output of the defective slice array, wherein the remap selector
19 circuit associated with each slice array comprises an OR gate, wherein
20 the OR gate has a first OR-gate input, a second OR-gate input, and an
21 OR-gate output, wherein the first OR-gate input is connected to the
22 OR-gate output associated with the adjacent higher-numbered slice
23 array, wherein the second OR-gate input is connected to the output of

28 the remap register, and wherein the OR-gate output is connected to the
input of the write selector circuit and the read selector circuit.

Claim 4 (Previously Presented):

2 An electronic circuit for self-repair of a random access memory array,
comprising:

4 a write selector circuit associated with each slice array, wherein the
random access memory is organized into a plurality of slice arrays,
6 wherein each slice array comprises at least one memory storage cell,
and wherein at least one of the slice arrays is redundant;

8 a read selector circuit associated with each slice array;

10 a remap selector circuit associated with each slice array; and

12 a remap register associated with each slice array, wherein when power
14 is applied to the circuit, the circuit automatically performs a self-test,
wherein when the self-test detects a defect, the remap register of the
16 slice array having the defect is set to indicate the presence of the defect
resulting in the associated remap selector circuit instructing the
18 associated write selector circuit to redirect data intended for storage in
that slice array to an adjacent slice array and instructing the associated
20 read selector circuit to redirect data read from the adjacent slice array
to the output of the defective slice array, wherein the write selector
22 circuit associated with each slice array comprises a write multiplexer,
wherein the write multiplexer has a first write-multiplexer input, a
24 second write-multiplexer input, a write-multiplexer control input, and a
write-multiplexer output, wherein the write-multiplexer control input is
26 connected to the output of the remap selector circuit, wherein the first
write-multiplexer input is connected to the second write-multiplexer
28 input associated with the adjacent higher-numbered slice array,
wherein the second write-multiplexer input is connected to an output of
30 an input register, and wherein the write-multiplexer output is capable
of transferring data to the slice array.

Claim 5 (Previously Presented):

2 An electronic circuit for self-repair of a random access memory array,
comprising:

4 a write selector circuit associated with each slice array, wherein the
random access memory is organized into a plurality of slice arrays,
6 wherein each slice array comprises at least one memory storage cell,
and wherein at least one of the slice arrays is redundant;

8 a read selector circuit associated with each slice array;

10 a remap selector circuit associated with each slice array; and

12 a remap register associated with each slice array, wherein when power
14 is applied to the circuit, the circuit automatically performs a self-test,
16 wherein when the self-test detects a defect, the remap register of the
18 slice array having the defect is set to indicate the presence of the defect
20 resulting in the associated remap selector circuit instructing the
22 associated write selector circuit to redirect data intended for storage in
24 that slice array to an adjacent slice array and instructing the associated
26 read selector circuit to redirect data read from the adjacent slice array
28 to the output of the defective slice array, wherein the read selector
30 circuit associated with each slice array comprises a read multiplexer,
wherein the read multiplexer has a first read-multiplexer input, a
second read-multiplexer input, a read-multiplexer control input, and a
read-multiplexer output, wherein the read-multiplexer control input is
connected to the output of the remap selector circuit, wherein the first
read-multiplexer input is capable of obtaining data from the slice array,
wherein the second read-multiplexer input is connected to the first
read-multiplexer input associated with the adjacent lowered-numbered
slice array, and wherein the read-multiplexer output is capable of
transferring data to an output register.

Claim 6 (Previously Presented):

2 The electronic circuit as recited in claim 3, wherein the electronic
4 circuit is embedded within a bit-slice in an integrated circuit, wherein
the bit-slice comprises the slice array and other circuitry associated
with the slice array.

Claim 7 (Previously Presented):

2 The electronic circuit as recited in claim 3, wherein when the defect is
present:
4 for each slice array subsequent to the slice array in which the defect is
6 present, the remap selector circuit instructs the write selector circuit to
redirect data intended for storage in that slice array to its adjacent slice
8 array, and
10 for each slice array subsequent to the slice array in which the defect is
12 present, the remap selector circuit instructs the read selector circuit to
redirect data read from its adjacent slice array to the output of the slice
array,

Claim 8 (Previously Presented):

2 The electronic circuit as recited in claim 3, wherein the electronic
circuit is an integrated circuit.

Claim 9 (Cancelled):

Claim 10 (Previously Presented):

2 The electronic circuit as recited in claim 4, wherein when the self-test
detects that one of the slice arrays is defect free, the remap register
4 associated with that slice array is set to indicate that the slice array is
defect free resulting in the associated remap selector circuit instructing
6 the associated write selector circuit to direct data intended for storage
in that slice array to that slice array and instructing the associated read
8 selector circuit to direct data read from that slice array to the output of
that slice array.

Claim 11 (Previously Presented):

2 The electronic circuit as recited in claim 4, wherein the electronic
circuit is embedded within a bit-slice in an integrated circuit, wherein
4 the bit-slice comprises the slice array and other circuitry associated
with the slice array.

Claim 12 (Previously Presented):

2 The electronic circuit as recited in claim 4, wherein when the defect is
present:
4 for each slice array subsequent to the slice array in which the defect is
present, the remap selector circuit instructs the write selector circuit to
6 redirect data intended for storage in that slice array to its adjacent slice
array, and
8 for each slice array subsequent to the slice array in which the defect is
10 present, the remap selector circuit instructs the read selector circuit to
redirect data read from its adjacent slice array to the output of the slice
12 array,

Claim 13 (Previously Presented):

2 The electronic circuit as recited in claim 4, wherein the electronic
circuit is an integrated circuit.

Claim 14 (Previously Presented):

2 The electronic circuit as recited in claim 5, wherein when the self-test
detects that one of the slice arrays is defect free, the remap register
4 associated with that slice array is set to indicate that the slice array is
defect free resulting in the associated remap selector circuit instructing
6 the associated write selector circuit to direct data intended for storage
in that slice array to that slice array and instructing the associated read
8 selector circuit to direct data read from that slice array to the output of
that slice array.

Claim 15 (Previously Presented):

2 The electronic circuit as recited in claim 5, wherein the electronic
circuit is embedded within a bit-slice in an integrated circuit, wherein
4 the bit-slice comprises the slice array and other circuitry associated
with the slice array.

Claim 16 (Previously Presented):

2 The electronic circuit as recited in claim 5, wherein when the defect is
present:
4 for each slice array subsequent to the slice array in which the defect is
present, the remap selector circuit instructs the write selector circuit to
6 redirect data intended for storage in that slice array to its adjacent slice
array, and
8
10 for each slice array subsequent to the slice array in which the defect is
present, the remap selector circuit instructs the read selector circuit to
12 redirect data read from its adjacent slice array to the output of the slice
array,

Claim 17 (Previously Presented):

2 The electronic circuit as recited in claim 5, wherein the electronic
circuit is an integrated circuit.